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PATENT
Attorney Docket No.: DB000575-015

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	)	
		)	**Examiner:** Not yet assigned
Serial No.:	Not yet assigned	)	
		)	**Art Unit:** Not yet assigned
Filed:	6 July 2001	)	

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

PRELIMINARY AMENDMENT

Preliminary to the examination of the above-identified application filed herewith, please amend that application as follows.

In the Specification

Page 1, line 2, after the title, insert -- This Application is a continuation application of U. S. Application Serial No. 09/621,012 filed July 20, 2000, which is a divisional application of U.S. Application Serial No. 08/916,692 filed August 22, 1997.--

Page 52, line 18, delete "nine microfiche having a total of fifty-two frames" and substitute therefore --eleven microfiche having a total of sixty-six frames--.

Page 52, line 19, delete "33" and substitute therefore --44--.

A replacement page 52 is enclosed; a copy of page 52 marked to show the changes is also enclosed.

In the claims

Please cancel claims 1-69, 72-99, 101-119, 121-125, 127-134, 137, 144-146, 148-151, 153-159, and 166.

STATEMENT REQUESTING DELETION OF INVENTORS

The declaration that is being filed with the instant application is a copy of the declaration that was filed with U.S. Application Serial No. 08/916,692 filed August 22, 1997. As a result of the restriction requirement in U.S. Application Serial No. 08/916,692, the following inventors named in the grandparent application are not inventors of the invention claimed in the instant divisional application:

Scott J. Derner
Larry D. Kinsman
Ronald Taylor
John Mullin

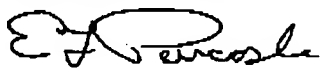
Please file the instant application in the names of the remaining inventors (Keeth, Bunker, Beffa and Ross) in accordance with 37 CFR 1.63 (d).

CHANGE OF ADDRESS

Please note that the undersigned attorney's address has changed since the parent application was filed and that the undersigned attorney's address is correctly noted on form PTO/SB/05 filed herewith, and is correctly noted below.

It is respectfully requested that the instant application, covering claims 70, 71, 100, 120, 126, 135, 136, 138-143, 147, 152, 160-165 receive an early office action on the merits.

Respectfully submitted



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PATENT
Attorney Docket No.: DB000575-005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	)	
		)	**Examiner:**
Serial No.:	Not yet assigned	)	
		)	**Art Unit:**
Filed:	20 July 2000	)	

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

PRELIMINARY AMENDMENT

Preliminary to the examination of the above-identified application filed herewith, please amend that application as follows.

In the Specification

Page 1, line 2, after the title, insert – This application is a divisional application of U.S. Application Serial No. 08/916,692 filed August 22, 1997. - -

In the claims.

Please cancel claims 1 – 69 an 72 – 80 and add the following new claims.

--81. The memory of claim 70 wherein said test mode logic is responsive to an all row high test condition.

82. The memory of claim 70 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

83. The memory of claim 82 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

84. The memory of claim 83 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

85. The memory of claim 84 wherein said multiplexers are positioned at every second individual array.

86. The memory of claim 70 wherein said array of memory cells is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

87. The memory of claim 86 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

88. The memory of claim 86 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

89. The memory of claim 70 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

90. The memory of claim 89 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

91. The memory of claim 70 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

92. The memory of claim 91 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

93. The memory of claim 91 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

94. The memory of claim 70 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

95. The memory of claim 94 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

96. The memory of claim 70 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

97. The memory of claim 70 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

98. The memory of claim 70 wherein said memory provides at least 256 meg of storage.

99. The memory of claim 98 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

100. A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral device; and

test mode logic for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latch responsive to a first external signal when the memory is in the test mode, for latching data stored in a first group of memory cells, and a write enable circuit responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory cells.

101. The system of claim 100 wherein said test mode logic is responsive to an all row high test condition.

102. The system of claim 100 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

103. The system of claim 102 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said

sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

104. The system of claim 103 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

105. The system of claim 104 wherein said multiplexers are positioned at every second individual array.

106. The system of claim 100 wherein said array of memory cells is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

107. The system of claim 106 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

108. The system of claim 106 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

109. The system of claim 100 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus

including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

110. The system of claim 109 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

111. The system of claim 110 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

112. The system of claim 111 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

113. The system of claim 111 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate or concurrent operation to achieve a predetermined level of output power.

114. The system of claim 100 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

115. The system of claim 114 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said

secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

116. The system of claim 100 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

117. The system of claim 100 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

118. The system of claim 100 wherein said memory provides at least 256 meg of storage.

119. The system of claim 118 wherein said array provides more than 256 meg of storage. said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

120. A combination for use in a memory having an array of memory elements, said combination comprising:

test mode logic for determining whether the memory is in a test mode;

a latch responsive to a first external signal when the memory is in the test mode, for latching data stored in a first group of memory elements; and

a write enable circuit responsive to a second external signal when the memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

121. The combination of claim 120 wherein said first external signal includes a row address strobe signal.

122. The combination of claim 120 wherein said second external signal includes a column address strobe signal.

123. The combination of claim 120 wherein said write enable circuit is responsive to a plurality of changes in state of the second external signal for enabling the latched data to be written to a plurality of groups of memory elements, respectively.

124. The combination of claim 123 wherein each of said groups of memory elements includes approximately twenty five percent of the memory elements.

125. The combination of claim 124 wherein said second external signal includes a column address strobe signal.

126. A method of writing to a plurality of memory elements, comprising the steps of:

writing known data into a first group of memory elements;

latching the data from the first group of memory elements in response to a first external signal; and

writing the latched data into a second group of memory elements in response to a second external signal.

127. The method of claim 126 wherein the first external signal is a row address signal and the second external signal is a column address strobe signal.

128. The method of claim 126 additionally comprising the steps of writing the latched data into a another group of memory elements each time the second external signal changes states.

129. The method of claim 128 wherein said first group of memory elements includes a row of memory elements and wherein said second and subsequent groups of memory elements each include approximately twenty five percent of the memory elements.

130. The method of claim 126 wherein said step of latching the data includes the step of connecting each memory element in the first group to one of a plurality of sense amps.

131. The method of claim 130 wherein said step of connecting each memory element includes the step of biasing a plurality of isolation transistors into conductive states to connect each memory element in said first group to one of the sense amps.

132. The method of claim 131 wherein said step of writing the latched data into a second group of memory elements includes the step of connecting each memory element in the second group to one of the sense amps.

133. The method of claim 132 wherein said step of connecting each memory element in the second group includes the step of biasing a plurality of isolation transistors into conductive states to connect each memory element in the second group to one of the sense amps.

134. The method of claim 71 additionally comprising the steps of:

writing the latched data into a second group of memory elements in response to a change in state of the second external signal;

writing the latched data into a third group of memory elements in response to another change in state of the second external signal; and

writing the latched data into a fourth group of memory elements in response to a further change in state of the second external signal.

135. A method of testing a portion of a memory array having a plurality of memory elements formed in a plurality of rows, and wherein said array is arranged in a plurality of memory blocks, said method comprising the steps of:

selecting a memory block for testing:

writing test data into a first row of memory elements in the selected memory block;

latching the test data from the first row of memory elements in response to a first external signal;

writing the latched test data into a first plurality of rows of memory elements in response to a second external signal;

reading the test data from the memory block; and

comparing the test data read from the memory block with the test data written into the first row.

136. The method of claim 135 wherein the first external signal is a row address strobe signal and the second external signal is a column address strobe signal.

137. The method of claim 136 additionally comprising the steps of writing the latched data into another plurality of rows each time the column address strobe signal changes state.

138. A method, comprising:

inputting to a solid state device a voltage outside the range of voltages used to represent logic signals;

inputting at least one address to the device; and

decoding the address to ascertain test mode information.

139. The method of claim 138 wherein the step of inputting the voltage includes the step of inputting a voltage higher than the highest voltage used to represent logic signals in the device.

140. The method of claim 138 wherein said step of inputting at least one address to the device is performed while the step of inputting a voltage is being performed.

141. The method of claim 140 additionally comprising the step of decoding the address information to ascertain if the test mode information includes instructions to test for the presence of the voltage outside the range of voltages used to represent logic signals in the device.

142. A method of placing a solid state device into a mode in which it is capable of receiving test mode information, comprising:

inputting to the device a voltage outside the range of voltages used to represent logic signals;

enabling a detector; and

confirming with said detector the presence of the voltage outside the range of voltages used to represent logic signals.

143. A method of inputting test mode information to a solid state device, comprising:

inputting to the device a voltage outside the range of voltages used to represent logic signals;

enabling a detector;

confirming the presence of the voltage outside the range of voltages used to represent logic signals; and

inputting to the device at least one address containing test mode information.

144. The method of claim 143 wherein said step of enabling a detector is performed by the steps of inputting a first address and a sequence of control signals.

145. The method of claim 143 wherein said step of inputting at least one address to the device is performed while said step of inputting a voltage is performed.

146. The method of claim 143 additionally comprising the step of inhibiting the device from normal operation while said step of inputting a voltage is performed.

147. A method of placing a solid state device into a test mode, comprising:

applying to the device a voltage outside the range of voltages used to represent logic signals, and while said voltage is being applied;

inputting at least two addresses to said device, said first address containing information used to confirm the presence of said voltage outside the range of voltages used to represent logic signals, and said second address containing information used to place the device into a test mode.

148. The method of claim 147 wherein the step of applying a voltage includes the step of applying a voltage higher than the highest voltage used to represent logic signals in the device.

149. The method of claim 147 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

150. The method of claim 147 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

151. The method of claim 147 additionally comprising the step of inputting an address containing information to take the device out of a test mode.

152. A method of placing a solid state memory device into a test mode, comprising:

applying to the device a voltage outside the range of voltages used to represent logic signals, and while said voltage is being applied;

applying a specific combination of control signals to enable the receipt of a test enable key;

verifying the test enable key and confirming the presence of the applied voltage;

applying said specific combination of control signals to enable the receipt of at least one test mode key; and

decoding the test mode key to place the device in a test mode.

153. The method of claim 152 wherein the specific combination of control signals includes the assertion of the write signal followed by the assertion of the column address strobe and row address strobe signals.

154. The method of claim 152 wherein the step of applying a voltage includes the step of applying a voltage higher than the highest voltage used to represent logic signals in the device.

155. The method of claim 152 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

156. The method of claim 152 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

157. The method of claim 152 additionally comprising the step of inputting a clear test mode key to take the device out of a test mode.

158. The method of claim 152 wherein said test mode keys are received as address information on column address lines.

159. The method of claim 152 additionally comprising the steps of performing the test specified by the test mode key and outputting the test results.

160. A test logic circuit for a solid state memory device, comprising:

a test mode enable circuit for determining if a voltage outside the range of voltages used to represent logic levels is being applied to the memory device under predetermined conditions; and

a circuit for receiving and decoding test mode keys in response to said test mode enable circuit.

161. The test logic circuit of claim 160 additionally comprising a test mode reset circuit for resetting said circuit for receiving and decoding test mode keys.

162. The test logic circuit of claim 160 additionally comprising a circuit for inhibiting said solid state memory device from normal operations when the device is in a test mode.

163. A solid state memory device, comprising:

a plurality of memory cells;

a plurality of peripheral devices for writing information into and reading information out of said memory cells; and

a test logic circuit, comprising:

a test mode enable circuit for determining if a voltage outside the range of voltages used to represent logic levels is being applied to the memory device under predetermined conditions; and

a circuit for receiving and decoding test mode keys in response to said test mode enable circuit;

said memory device further comprising circuits, responsive to said decoded test mode keys, for performing tests on at least one of said memory cells and peripheral devices.

164. The memory device of claim 163 wherein said test mode enable circuit includes logic for receiving a row address strobe signal (RAS), a write column address strobe before RAS signal, the applied voltage, and certain address information on column address lines and for producing therefrom a latch signal.

165. The memory device of claim 164 additionally comprising a test mode reset circuit for resetting said circuit for receiving and decoding test mode keys.

166. The memory device of claim 165 wherein said test mode reset circuit includes logic for receiving a row address strobe signal (RAS), a column address strobe signal (CAS), a write CAS before RAS signal and for producing therefrom a test mode reset signal and a super voltage test mode reset signal. --

REMARKS

The instant amendment presents new claims 81 – 166 for examination. No new matter has been added by claims 81 – 166.

STATEMENT REQUESTING DELETION OF INVENTORS

As a result of the restriction requirement, the following inventors named in the parent application are not inventors of the invention claimed in the instant divisional application:

Scott J. Derner
Larry D. Kinsman
Ronald Taylor
John Mullin

Please file the instant application in the names of the remaining inventors (Keeth, Bunker, Beffa and Ross) in accordance with 37 CFR 1.63 (d).

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Respectfully submitted

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Dated: 20 July 2000